Notice of Allowability	Application No.	Applicant(s)	
	10/757,464	HUANG ET AL.	
	Examiner	Art Unit	
	Shane M. Thomas	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *Amendment filed 6/7/2006*.

2. ☒ The allowed claim(s) is/are *1-21*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☒ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☒ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date 20060907.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

EXAMINER'S AMENDMENT

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Alun L. Palmer (Reg. No. 47,838) on 9/7/2006.

The application has been amended as follows:

Lines 3-30 of page 7 have been replaced to read:

Fig. 4 is a diagram of the architecture of flash ROMs according to the embodiment of the invention. The apparatus 300 manages two types of flash ROM, LPC flash ROM 41 and firmware hub flash ROMs 42 to 45, compatible with low pin count interface specification revision 1.1 (LPC 1.1). The apparatus 300 is designed to enable access to both types of flash ROM to reduce costs. It is noted that only ~~on~~ one type of flash ROM is disposed on one motherboard. Preferably, only one ROM is provided to store the basic input/output system (BIOS) when the LPC flash ROM is disposed. However, multiple ROMs of various sizes can be provided to respectively store system BIOS, super I/O or network card data when the firmware hub flash ROM is disposed.

Fig. 5 is a diagram of an exemplary address record according to the embodiment of the present invention. The storage device 301 contains four address records, in which the item numbers range from 0 to 3, and correspond to firmware hub flash ROMs 42 to 45. The firmware

hub flash ROM 42, referring to the BIOS flag 1 when the IDESEL is 0, stores a system BIOS required to boot the system, occupies 512K of address space between FFF8_0000H and FFFF_FFFFH. The firmware hub flash ROM 43, referring to the BIOS flag 1 when the IDESEL is 1, occupies 512K of address space ranging from FFF0_0000H to FFF7_FFFFH, and stores the redundant system BIOS for system BIOS recovery. The keyboard mapping matrix data fort the embedded KBC controller is stored in the firmware hub

Lines 1-19 of page 9 have been replaced to read:

Fig. 7 is a flowchart showing a method of firmware hub flash ROM selection according to the embodiment of the invention. The apparatus 300 includes a storage device 301 storing multiple address records associated with firmware hub flash ROMs. First, the address record is set ~~as~~ at step S71. In step S72, the process unit 301 receives the signal output from the strapping component and a memory access request with an access range from the CPU 310. As in S731, when the signal is "on" meaning only one LPC flash ROM is disposed, it accesses the LPC flash ROM, and preferably reads the system BIOS to reboot the system according to the access range. In S732, when the strapping component is set to "off" and the access range corresponds to range 0, it controls the firmware hub flash ROM, and preferably reads system BIOS, with "IDSEL" number 0. Otherwise, in S733, and S734, when the address range corresponds to range 1 or range 2, it controls the firmware hub flash ROM with "IDSEL" number 1 or 2.

Claim 20 has been amended (to remove an errant underscore in line 4) to read:

20. A flash ROM management apparatus, comprising:

at least one flash ROM corresponding to one of a plurality of flash ROM types;

a strapping component, configured to output a signal indicating the flash ROM type corresponding to the flash ROM before conducting power on self test (POST) procedure; and

a process unit, coupled to the flash ROM and the strapping component, receiving a memory access request with an access range from the a CPU, receiving the signal, acquiring the flash ROM type according to the signal, and executing an LPC 1.1 memory access instruction with the access range corresponding to a memory cycle corresponding to the flash ROM type.

Drawings

The following changes to the drawings have been approved by the examiner and agreed upon by applicant: Figure 8, step S82 should be amended to remove the typographical errors contained therein and read "Receiving signal outputted from strapping component". In order to avoid abandonment of the application, applicant must make these above agreed upon drawing changes.

Notice of Allowance

Remarks

Prosecution of this case has been assumed by Examiner Shane Thomas. As per MPEP §704.01, the prior examiner's search has been given full faith and credit. An updated search has been performed by the present Examiner yielding additional prior art to be made of record; however, as discussed herein below, the prior art made of record does not specifically teach Applicant's invention as defined by the claims.

Reasons for Allowance

Claims 1-21 are allowable over the prior art of record.

The following is an examiner's statement of reasons for allowance:

Applicant's amendment and arguments (pages 8-11 of the response) filed 6/27/2006 have overcome all outstanding rejections. The Examiner agrees with the arguments presented by the Applicant in that the prior art references of Shahar et al., Gulick et al., and Kao, do not teach, either alone or in combination, the entirety of Applicant's independent claims 1,11, and 20.

Chang et al. (U.S. Patent Application Publication No. 2003/0182495) teaches a detection circuit (figure 2) that determines the type of flash ROM (FirmWare Hub or Low Pin Count) installed on the system in order to determine perform the correct memory cycle when accessing the specific ROM. Chang does not teach the ROM being a LPC revision 1.1 type ROM and does not teach the system having a storage device having multiple address records comprising a unique address range and identity associated with each of a plurality of flash ROM types.

Poisner (U.S. Patent Application Publication No. 2002/0049880) teaches using an incoming address portion to determine which portion of a Low Pin Count (LPC) device to access; however, Poisner does not teach the device being an LPC revision 1.1 compliant device, nor teaching the system having a storage device having multiple address records comprising a unique address range and identity associated with each of a plurality of flash ROM types.

Hongo et al. (U.S. Patent No. 5,592,652) teaches multiple ROM devices - external ROM 32 and internal ROM 22 (figure 1) - as well as a storage device 9 (figure 7) that comprises address records 9a-9d of address ranges associated with the ROMs 22 and 32. A strapping component 8 outputs a signal based on the particular flash ROM type (internal or external) to be accessed based on an incoming memory access request's --access range--. Hongo, however, does not specifically teach the system being able to execute an LPC Revision 1.1 type memory instruction corresponding to a memory cycle nor the storage device 9 additionally comprising an --identity-- associated with each of the plurality of flash ROMs and the corresponding address ranges - the identity element being used to access a corresponding flash ROM once a match between the incoming access range and one of the address ranges occurs.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shane M. Thomas whose telephone number is (571) 272-4188. The examiner can normally be reached on M-F 8:30 - 5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt M. Kim can be reached on (571) 272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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